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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,712	11/17/2003	Michael D. Gallant	03-1040 1496.00344	2328

24319 7590 01/15/2008

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EXAMINER	
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ART UNIT	PAPER NUMBER
2621	

MAIL DATE	DELIVERY MODE
01/15/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/714,712	GALLANT ET AL.	
	Examiner	Art Unit	
	David N. Werner	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-7,9-11,13-16 and 19-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-7,9-11,13-16 and 19-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 May 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action for US Patent Application 10/714,712 is in response to the Request for Continued Examination filed 12 November 2007, in reply to the Final rejection of 16 August 2007. Currently, claims 1, 2, 4-7, 9-11, 13-16, and 19-25 are pending.

2. In the previous Office action, claims 1, 10, 11, and 21-25 were rejected under 35 U.S.C. 103(a) as obvious over JP 2000-308064 A (Hanami et al.), claims 2, 4-6, and 20 were rejected under 35 U.S.C. 103(a) as obvious over Hanami et al. in view of US 6,455,642 B2 (Arcoleo et al.), and claims 7, 9, 13-16, and 19 were rejected under 35 U.S.C. 103(a) as unpatentable over Hanami et al. in view of EP 1,143,712 A2 (Topper). Claims 13-16 were objected to as being dependent on a later claim.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12 November 2007 has been entered.

Response to Arguments

4. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection. Applicant argues that Hanami et al. does not teach the claimed limitation of searching for motion vectors in an image in which a small offset is determined from a still region and a large offset is determined from a moving region. Hanami et al. teaches searching for motion vectors using multiple regions. In Hanami et al., a search range may depend on the degree of motion in am image (column 11: lines 51-57). However, in Hanami et al., search ranges are dependent on a current picture as a whole, not regions of the picture (column 4: lines 53-59).

5. Applicant's arguments filed with respect to claim 6 have been fully considered but they are not persuasive. Applicant argues that Hanami et al. does not teach "two circuits generating two address signals, one for reads and one for writes". It is respectfully submitted that this is not what is claimed in claim 6. Claim 6 of the present invention states, "The apparatus according to claim 5, wherein said first circuit further comprises an internal read control circuit configured to generate a second read address to read from said search memory". Claim 6 does not discuss a circuit that generates a write address signal. In addition, it is respectfully submitted that Hanami et al. teaches the limitations of claim 6. In Hanami et al., two reference picture memories 41 and 42 are used to store reference pictures, with the two memories storing different pictures (column 12: lines 55-56). If the current picture is a B picture, address generating circuit 55c generates different addresses for the two different pictures (column 15: lines 42-50). Therefore, the examiner respectfully maintains the rejection of claim 6.

6. Applicant's arguments filed with respect to claim 16 have been fully considered but they are not persuasive. Applicant argues that Topper et al. does not teach the claimed limitation of a motion vector search spanning three different sets of reference sample copied from a memory and a set of last reference samples partially overwriting a set of initial reference samples. It is respectfully submitted that this statement is in error. Recall the prior analysis of parent claim 19, in which figure 3B of Topper et al. was relied on for claim mapping. Motion vector 222 for block 220 is generated from block 212, and motion vector 314 for block 312 is generated from block 310, which overlaps block 212 by four horizontal pixels (paragraphs 0023-0027). Block 310 corresponds with the claimed "third reference samples", motion vector 314 corresponds with the claimed "third motion vector", and block 312 corresponds with the claimed "second current block". The portion of block 310 that overlaps with block 212 corresponds with the claimed "first portion of said first reference samples". In a similar manner, figure 4B of Topper et al. shows the generation of an additional motion vector for a third block (paragraphs 0028-0029). Motion vector 414 corresponds with th claimed "fourth motion vector", block 412 corresponds with the claimed "third current block", and block 410 corresponds with the claimed "fourth reference samples". The portion of blocks 212, 310, and 410 that overlap corresponds with the claimed "fourth reference samples, said third reference samples, and at least a second portion of said first reference samples". Therefore, the examiner respectfully maintains the rejection of claim 16.

Claim Objections

7. The objection of claims 13-16 under 37 CFR 1.75(c) as being of improper dependent form for failing to further limit the subject matter of a previous claim is held in abeyance until allowable subject matter is indicated. See 37 CFR 1.126.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 10, 11, and 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Japanese Patent Application 2000-308064 (Hanami et al.), relying on corresponding US Patent 6,765,965 B1 for translation, in view of US Patent 6,456,660 B1 (Yokoyama). Hanami et al. teaches a motion vector detection apparatus that divides a search into parallel sub-units. Regarding claim 1, figure 13 illustrates a configuration of the apparatus of Hanami et al. In this embodiment, reference picture memories 41 and 42 store reference pictures (column 12: line 55–column 13: line 14). This corresponds with the claimed memory. Also in Hanami et al., a plurality of motion detecting circuits MD #X each receive portions of the contents of reference picture memories 41 and 42 through buffers 43-48. This plurality of motion detecting circuits corresponds with the claimed first and second circuits. The motion detecting circuits each generate a motion vector for a "template block" in a current frame. If the current

frame is a P-frame, the motion detecting circuits search different offset windows of the same reference frame (column 10: line 65–column 11: line 25).

One difference between Hanami et al. and the present invention is that in Hanami et al., pixel offsets for a reference frame are measured with respect to a current macroblock, and in the present invention, pixel offsets for a reference frame are measured relative to a corner of the reference frame. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to set the origin of an offset measurement of a reference image from a corner of the reference image rather than a current macroblock, since the examiner takes Official Notice of the equivalence of determining an offset relative to **any** point in a given image for its use in measuring additional relative distances from said point. It would have been well within the level of ordinary skill of the art at the time the invention was made, for instance, to determine the location of the current template block as an offset from a corner of the reference frame.

The other difference between Hanami et al. and the present invention is that in the present invention, search areas are generated according to the motion of different regions of a current image, and in Hanami et al., the size of a search range may depend on the degree of motion in am image as a whole, (column 4: lines 54-59; column 11: lines 51-57).

Yokoyama teaches a motion vector detection system. Regarding claim 1, in Yokoyama et al., a motion vector detection means divides an image into several regions, and determines a search range based on the motion of each region (column 3:

lines 27-41). Figure 1 of Yokoyama et al. shows an embodiment of the invention, with motion vector detection section 103. This section divides an input image 101 and a reference image 102 into regions, and determines the motion vectors for each of the regions according to the search ranges determined by search range section 108 (column 6: lines 56-65). The motion vectors of the regions of the frame are entered into a histogram (column 10: lines 1-14), and so the search range for the next frame is shifted in the direction of the most common non-zero motion vectors (column 10: lines 15-35). Although Yokoyama decreases the weight of still regions that produce a zero motion vector, a largely still image may still be given a shift of (0, 0).

Hanami et al. discloses a majority of the claimed invention except for determining the offset of a motion search based on motion of regions in an image. Yokoyama teaches that it was known to set an offset of a motion vector search according to the most common motion vector of the regions of an image. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to offset the search ranges of Hanami et al. according to the motion of regions in an image, as taught by Yokoyama, since Yokoyama states in column 3: lines 12-19 that such a modification would reduce the complexity of a motion detector search apparatus.

Regarding claim 11, in Hanami et al., each motion detecting circuit MD #X copies a different search window of a reference image from one of the reference picture memories and generates a motion vector corresponding to the current template block from the appropriate search window, corresponding with steps A-D of the present invention, and Yokoyama performs a method of dividing an image into regions and

determining a motion vector search range from the motion vector distribution of the regions (claim 13), corresponding with step D of the present invention.

Regarding claims 10 and 23, in Hanami et al., if the current frame is a B-frame, two motion detecting circuits may search for motion vectors in a distant frame, and a third motion detecting circuit may search for a third motion vector in a near frame, as illustrated in figure 12. Note that the three search windows all have different offsets relative to the current template block (column 11: lines 26-57). Regarding claims 21 and 25, in Yokoyama, a still region produces an offset of (0, 0), although the effect of this is de-weighted for determining the search ranges for complex images (column 4: lines 40-50). Regarding claim 22, in Hanami et al., control circuit 55 controls all memory reads and writes for current picture memory 40, reference picture memories 41 and 42, and buffer memories 43-48 (column 14: line 8–column 15: line 55). Regarding claim 24, in Hanami et al., if the current picture is a B-picture, as illustrated in figure 7B, then the motion detecting circuits may be divided into two groups: group DGB, which performs backwards prediction, and group DGF, which performs forward prediction (column 9: lines 51-64).

Claims 2, 4-6, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hanami et al. in view of Yokoyama as applied to claim 1 above, and further in view of US Patent 6,445,645 B2 (Arcoleo et al). Regarding claim 2, figure 13 of Hanami et al. illustrates buffer memories 43-48 that copy selected references from the reference picture memories 41 and 42 (column 11: line 67–column 12: line 9). Each buffer stores

only the reference data corresponding with the pixels for the search area for its corresponding motion detector circuit (column 13: lines 15-30), and so corresponds with the claimed "search memory". Although Hanami et al. shows the buffers as separate components from the motion detector circuits, it would have been obvious to one having ordinary skill in the art at the time the invention was made to integrate these buffers with the motion detector circuits, since it has been held that forming in one piece an article which has been formerly been formed in two pieces and put together involves only routine skill in the art. See *Howard v. Detroit Stove Works*, 150 U.S. 164 (1893).

Although figure 13 of Hanami et al. demonstrates a set of lines connecting the buffer memories and the picture reference memories and a separate set of lines connecting the buffer memories and the motion detector circuits, applicant contends that this is not sufficient to demonstrate a write port separate from a read port in a memory. Arcoleo et al. teaches a random access memory with a separate read port and write port (abstract). Regarding claim 2, figure 2 of Arcoleo et al. illustrates an embodiment of this invention. Data enters, or is written to, through bus DIN[17:0] (column 4: line 60), and leaves, or is read from, through bus DOUT[17:0] (column 5: line 41).

Hanami et al., in combination with Yokoyama, discloses the claimed invention except, allegedly, a memory with a separate read port and write port. Arcoleo et al. teaches that it was known to provide a memory with an independent read port and write port. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide separate read and write ports to the buffers of

Hanami et al., as taught by Arcoleo et al., since Arcoleo et al. states in column 1, lines 27-30 that such a modification would permit synchronous reading to and writing from the buffer.

Regarding claims 4-6, in Hanami et al., control circuit 55 includes buffer memory read control circuit 55f controls reading from and writing to the buffer memories (column 14: lines 32-35). Address generating circuit 55c generates addresses to read from the reference frame memory (column 15: lines 36-50), and reference picture memory read control circuit 55e performs the actual read from the memory (column 14: lines 28-31). Buffer memory read control circuit 55f generates addresses for reading from the buffer memory (column 15: lines 51-55). Since when a current picture is a B picture, the two memories contain different pictures (column 12: lines 55-56), at least one distinct address must be generated for each memory (column 15: lines 43-48).

Claim 20 of the present invention is in proper means-plus-function format, and invokes 35 U.S.C. §112, sixth paragraph. Then the "means for searching" motion vectors and the "means for copying" reference samples from an external memory will be limited to a motion estimation processor circuit with a search memory and a control system, as described in the specification and shown in figure 4 of the present invention. Regarding claim 20, the motion detection circuits, buffer memories, control circuit, and reference picture memories of Hanami et al., when the buffer memories are modified in accordance with Arcoleo et al. as described above, fully encompass the subject matter of claim 20.

10. Claims 7, 9, 13-16, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hanami et al. in view of Yokoyama as applied to claims 1 and 11 above, and further in view of European Patent Application Publication 1,143,712 A2 (Topper). In one embodiment of Hanami et al., one motion detecting circuit determines motion vectors for a different template block than the other motion detecting circuits (column 16: lines 16-22). However, the search areas for the different motion detecting circuits do not overlap (column 16: lines 37-39), and so do not meet the claimed requirement of the search range for the second block including a portion of the search range for the first block.

Topper discloses a motion estimation system in which overlapping blocks are searched. Regarding claims 7 and 19, in the motion estimation method of Topper, large 8 x 8 blocks are searched, and the best-match motion vector is applied to a 4 x 4 sub-block at the center of the large block (paragraph 0025). Then, the large block corresponds with the "reference samples" and the sub-block corresponds with the "current block". Multiple overlapping large blocks are searched. In the example illustrated in figure 3B, a second block 310 overlaps first block 218 by four pixels horizontally. The motion vector for block 218 is applied to sub-block 220, and the motion vector for block 310 is applied to sub-block 312 (paragraph 0027).

Regarding claims 9 and 14, in Topper, the portion of second block 310 or third block 410 that does not overlap block 218 is adjacent to block 218 (figure 4B). Regarding claim 13, sub-block 220 is adjacent to sub-blocks 312 and 412 (figure 4B). Regarding claim 15, each time a new field is received in a current field memory in

Topper, the previous field is simultaneously transferred to a prior field memory, and a motion estimation processor generates motion vectors based on both the current field and the previous field (paragraph 0019). Regarding claim 16, the process of determining motion for a block horizontally adjoining a current block may be extended to a block vertically adjoining a current block (paragraphs 0028 and 0029). As shown in figure 4B, search ranges 212, 310, and 410, have some pixels in common.

Hanami et al., in combination with Yokoyama, discloses the claimed invention except for simultaneously searching for motion vectors for multiple blocks in overlapping search windows. Topper teaches that it was known perform multiple motion vector searches on overlapping areas of a frame. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the apparatus of Hanami et al. so that one of the motion detecting circuits would search for a motion vector for a second block in a search window overlapping the search window used by the other motion detecting circuits searching for a motion vector for a first block, as taught by Topper, since it was well-known to one having ordinary skill in the art at the time the invention was made that performing two independent processes, such as motion vector searches for two macroblocks, simultaneously, produces a faster result than performing them sequentially. This result, and its limit in performance gain, is commonly known as Amdahl's Law.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent 5,731,840 A (Kikuchi et al.) teaches a video coder and decoder that hierarchically divides an image into regions and determines a motion vector for each region. US Patent 6,563,874 B1 (Lu) teaches a motion estimator that divides an image into a foreground and a background. US Patent 6,985,527 B2 (Gunter et al.) teaches a motion estimation system that divides a video frame into regions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David N. Werner whose telephone number is (571) 272-9662. The examiner can normally be reached on Monday-Friday from 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mehrdad Dastouri can be reached on (571) 272-7418. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic

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DNW

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